AF/2634 IFW



# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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| In re application of: **Boerstler** | § | Group Art Unit: **2634** |
| Serial No.: **09/666,277** | § | Examiner: **Pathak, Sudhanshu C.** |
| Filed: **September 21, 2000** | § | Attorney Docket No.: **AUS9-2000-0240-US1** |
| For: **Method and System for Clock/Data Recovery for Self-Clocked High Speed Interconnects** | § | |

**Certificate of Mailing Under 37 C.F.R. § 1.8(a)**

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By: Amelia C Turner
Amelia C. Turner

35525

PATENT TRADEMARK OFFICE
CUSTOMER NUMBER

## TRANSMITTAL DOCUMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:
ENCLOSED HEREWITH:

- Appeal Brief (37 C.F.R. 41.37);
- Evidence as indicated in Evidence Appendix; and
- Our return postcard.

A fee of $340.00 is required for filing an Appeal Brief. Please charge this fee to IBM Corporation Deposit Account No. 09-0447. No additional fees are believed to be necessary. If, however, any additional fees are required, I authorize the Commissioner to charge these fees which may be required to IBM Corporation Deposit Account No. 09-0447. No extension of time is believed to be necessary. If, however, an extension of time is required, the extension is requested, and I authorize the Commissioner to charge any fees for this extension to IBM Corporation Deposit Account No. 09-0447.

Respectfully submitted,

Duke W. Yee

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Docket No. AUS9-2000-0240-US1 *PATENT*

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**Commissioner for Patents**
**P.O. Box 1450**
**Alexandria, VA 22313-1450**

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By: Amelia C. Turner
Amelia C. Turner

## APPEAL BRIEF (37 C.F.R. 41.37)

This brief is in furtherance of the Notice of Appeal, filed in this case on August 10, 2004.

The fees required under § 41.20(B)(2), and any required petition for extension of time for filing this brief and fees therefore, are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

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# REAL PARTY IN INTEREST

The real party in interest in this appeal is the following party: International Business Machines Corporation.

## RELATED APPEALS AND INTERFERENCES

With respect to other appeals or interferences that will directly affect, or be directly affected by, or have a bearing on the Board's decision in the pending appeal, there are no such appeals or interferences.

## STATUS OF CLAIMS

### A. TOTAL NUMBER OF CLAIMS IN APPLICATION

Claims in the application are: 1-50

### B. STATUS OF ALL THE CLAIMS IN APPLICATION

1. Claims canceled: NONE
2. Claims withdrawn from consideration but not canceled: NONE
3. Claims pending: 1-50
4. Claims allowed: 47-50
5. Claims objected to: 5, 6, 8, 9, 11, 13-34, and 38-46
6. Claims rejected: 1-4, 7, 10, 12, and 35-37

### C. CLAIMS ON APPEAL

The claims on appeal are: 1-4, 7, 10, 12, and 35-37

## STATUS OF AMENDMENTS

There are no amendments after final rejection.

## SUMMARY OF CLAIMED SUBJECT MATTER

The presently claimed invention provides a method, a signal recovery system, and a signal recovery circuit for a self-clocked transmission system where a received data signal is inputted to a first monostable circuit component **556** and a second monostable circuit component **558**. The first monostable circuit component generates a first output signal and the second monostable circuit component generates a second output signal. See specification, page 15, lines 9-28. The first output signal and the second output signal are compared using a first logical operator **580** to form a compared output signal, which is then provided as output. See specification, page 17, lines 9-27. More particularly, the monostable circuit components are "one-shot" circuit components. See specification, page 15, lines 9-28; page 17, lines 9-27. In an exemplary embodiment, the first logical operator is an OR gate. See specification, page 17, lines 9-27; element **580** in **Figure 5B**. An equalizer **512** is used to reduce distortion and to compensate for frequency dependent signal loss. The equalizer **512** provides input to the first monostable circuit component and the second monostable circuit component. See specification, page 15, lines 9-28. The equalizer may utilize the combination of a resistive-capacitive differentiator with gain and a comparator. See specification, page 18, line 30, to page 19, line 25; element **704** in **Figure 7**.

## GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The grounds of rejection on appeal are as follows:

Claims 1-3 and 7 are rejected under 35 U.S.C. § 102 as being anticipated by *van Driest et al.* (US Patent No. 5,003,562);

Claim 4 is rejected under 35 U.S.C. § 103 as being unpatentable over *van Driest* in view of *Kobayashi* (US Patent No. 6,028,461);

Claims 10, 35, and 36 are rejected under 35 U.S.C. § 103 as being unpatentable over *van Driest* in view of *Park* (US Patent No. 5,880,898);

Claim 12 is rejected under 35 U.S.C. § 103 as being unpatentable over *van Driest* in view of *Park* and further in view of *Streckmann et al.* (US Patent No. 4,535,299); and,

Claim 37 is rejected under 35 U.S.C. § 103 as being unpatentable over *van Driest* in view of *Park* and further in view of *Kobayashi.*

# ARGUMENT

## I. 35 U.S.C. § 102, Alleged Anticipation of Claims 1-3, and 7

The Final Office Action rejects claims 1-3 and 7 under 35 U.S.C. § 102 as being anticipated by *van Driest et al.* (US Patent No. 5,003,562). This rejection is respectfully traversed.

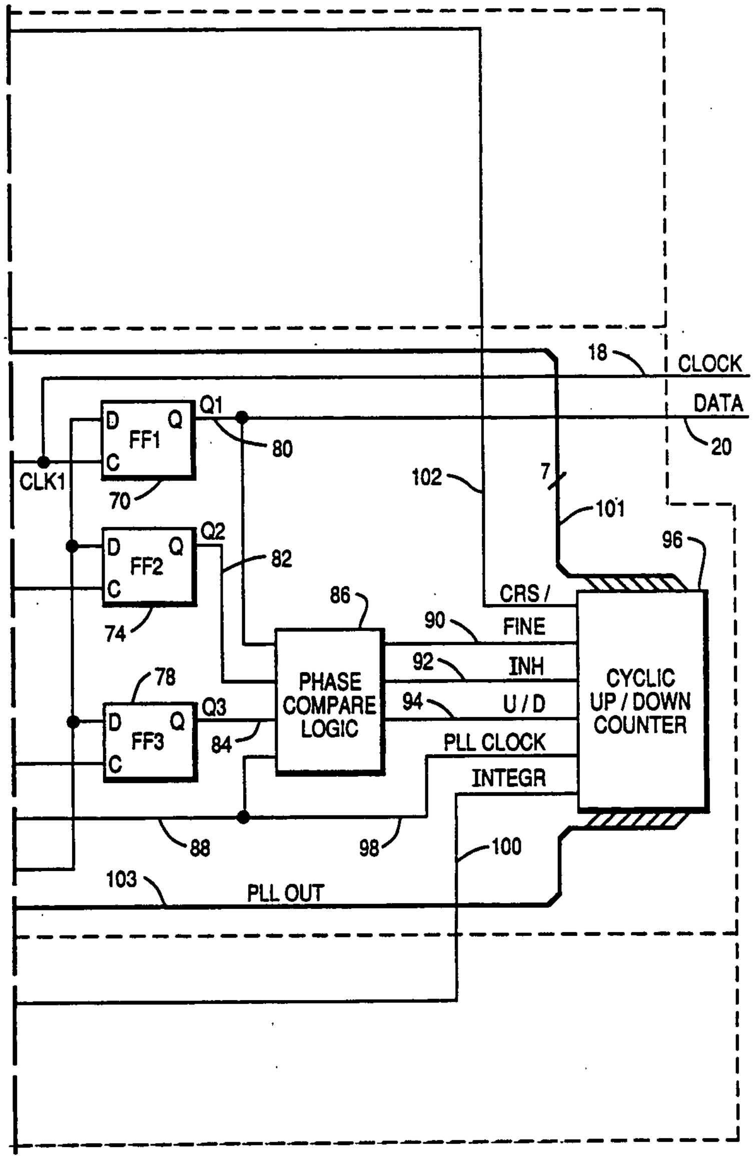
*Van Driest* teaches a digital phase lock loop decoder for use in decoding Manchester encoded data. The decoder includes a first sampling circuit for providing signals based on the clock speed of the encoded data, a delay circuit for generating delayed clock signals relative to the clock speed of the encoded data, a second sampling circuit for sampling the encoded data based on the delayed clock signal, a feedback circuit for generating clock signals whose phase corresponds with the phase of the delayed clock signals, and a storage for outputting decoded data signals corresponding to the encoded data utilizing the delayed clock signals. See *van Driest*, Abstract.

However, *van Driest* does not teach or suggest a first monostable circuit component and a second monostable circuit component, as recited in the instant claims. Claim 1 recites:

> 1. (Original): A signal recovery method for a self-clocked transmission system, comprising the steps of:
>
> inputting a received data signal to both a first monostable circuit component and a second monostable circuit component;
>
> generating a first output signal from the first monostable circuit component and a second output signal from the second monostable circuit component;
>
> comparing the first output signal and the second output signal to each other using a first logical operator; and
>
> outputting a compared output signal based on the comparison.

*Van Driest* does not teach or suggest "inputting a received data signal to both a first monostable circuit component and a second monostable circuit component," as recited in claim 1. The Final Office Action alleges that this feature is taught by elements **70** and **74** of **Fig. 3B**, which is reproduced as follows:

FIG. 3B




As clearly shown in **FIG. 3B** and as expressed in the corresponding description of *van Driest*, elements **70** and **74** depict conventional D-type flip-flops.

A person of ordinary skill in the art would readily recognize that a D-type flip-flop is a bistable circuit component and not a monostable circuit component, as alleged in the Office Action. In fact, a flip-flop is often referred to as a bistable multivibrator or a bistable trigger circuit, because the output of a flip-flop has two stable states, commonly referred to as a zero state and a one state. The *IBM Dictionary of Computing* defines "bistable" as follows:

> **bistable**. Pertaining to a device capable of assuming either of two stable states. (A)

The (A) designation indicates that this definition is taken from The *American National Standard Dictionary for Information Systems*, ANSI X3.172-1990, copyright 1990 by the American National Standards Institute (ANSI). The *IBM Dictionary of Computing* also defines "bistable trigger circuit" as follows:

> **bistable trigger circuit**. (1) A trigger circuit that has two stable states. (T) (2) Synonymous with flip-flop.

The (T) designation indicates that this definition is from The *Information Technology Vocabulary*, developed by Subcommittee 1, Joint Technical Committee 1, of the International Organization for Standardization and the International Electrotechnical Commision (ISO/IEC JTC1/SC1). See definitions from the *IBM Dictionary of Computing* (attached). Therefore, in other words, a D-type flip-flop is capable of holding two stable states, and is thus bistable. See also "4013 D-type flip-flops" from http://www.doctronics.co.uk/4013.htm (attached), which states that a D-type flip-flop is also called "a D-type bistable" and is a subsystem with **two stable states**. Also, a Wikipedia definition for "flip flop" states that a flip-flop is also referred to as a "bistable multivibrator." See http://en.wikipedia.org/wiki/Flip-flop (attached).

In contradistinction, independent claim 1, for example, recites "a first **monostable** circuit component" and "a second **monostable** circuit component." The *IBM Dictionary of Computing* defines "monostable" as follows:

> **monostable**. Pertaining to a device that has one stable state. (A)

Therefore, the claim clearly recites a first monostable circuit component and a second monostable circuit component that, by definition, have one stable state and *van Driest* clearly teaches only D-type flip-flops that, as well-known in the art, have two stable states and, thus, are bistable.

Furthermore, the present specification defines a monostable circuit component as follows:

> A monostable circuit component provides a pulse of known height and known width in response to a trigger signal.

*Van Driest* does not teach such a circuit component, because a D-type flip-flop generates an output signal that follows the input signal responsive to a trigger signal. As such, the flip-flop of *van Driest* merely provides an output that follows the input, rather than a pulse of known height

and known width. Therefore, *van Driest* does not teach or suggest "a first monostable circuit component" and "a second monostable circuit component," as recited in at least independent claim 1. In fact, the reference makes no mention whatsoever of the terms "monostable," "one-shot," or even "pulse."

The Final Office Action argues that *Haubner et al.* (U.S. Patent No. 4,459,591) discloses a monostable flip-flop as element **64** of **Figure 5** and as described in col. 9, lines 10-32. **Figure 5** is reproduced as follows:

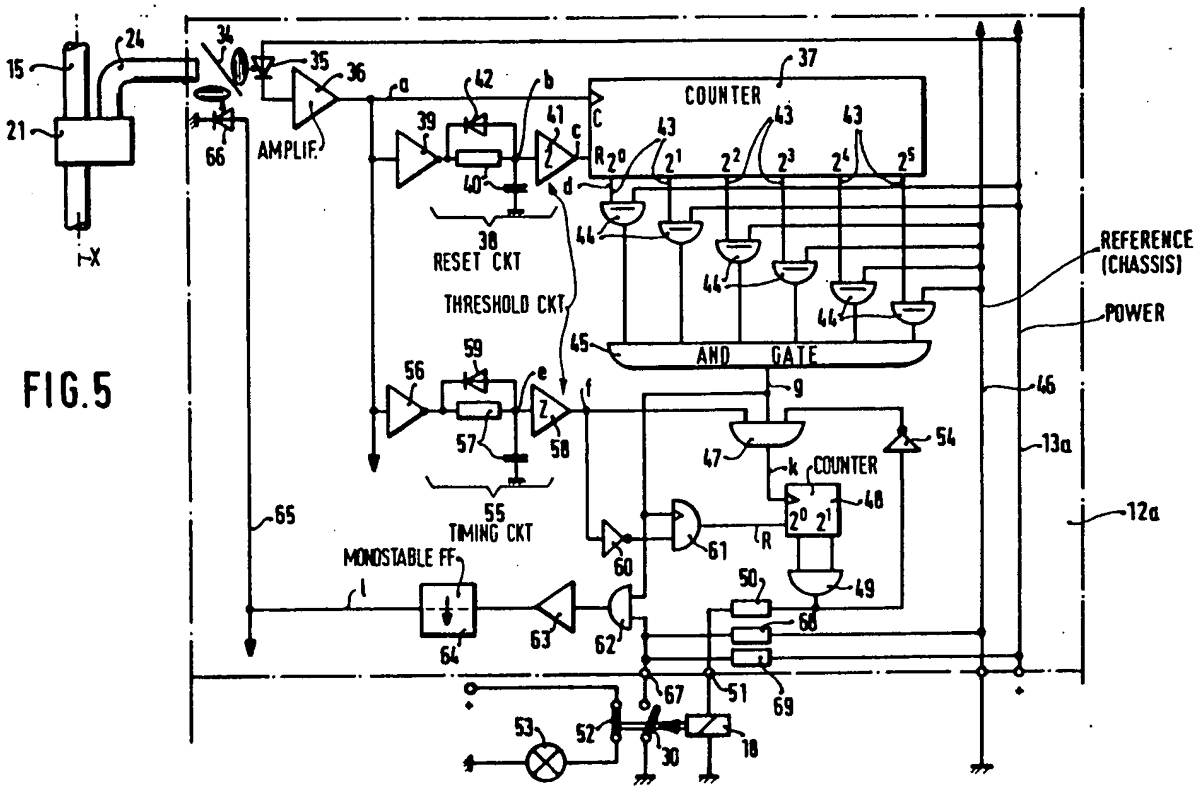


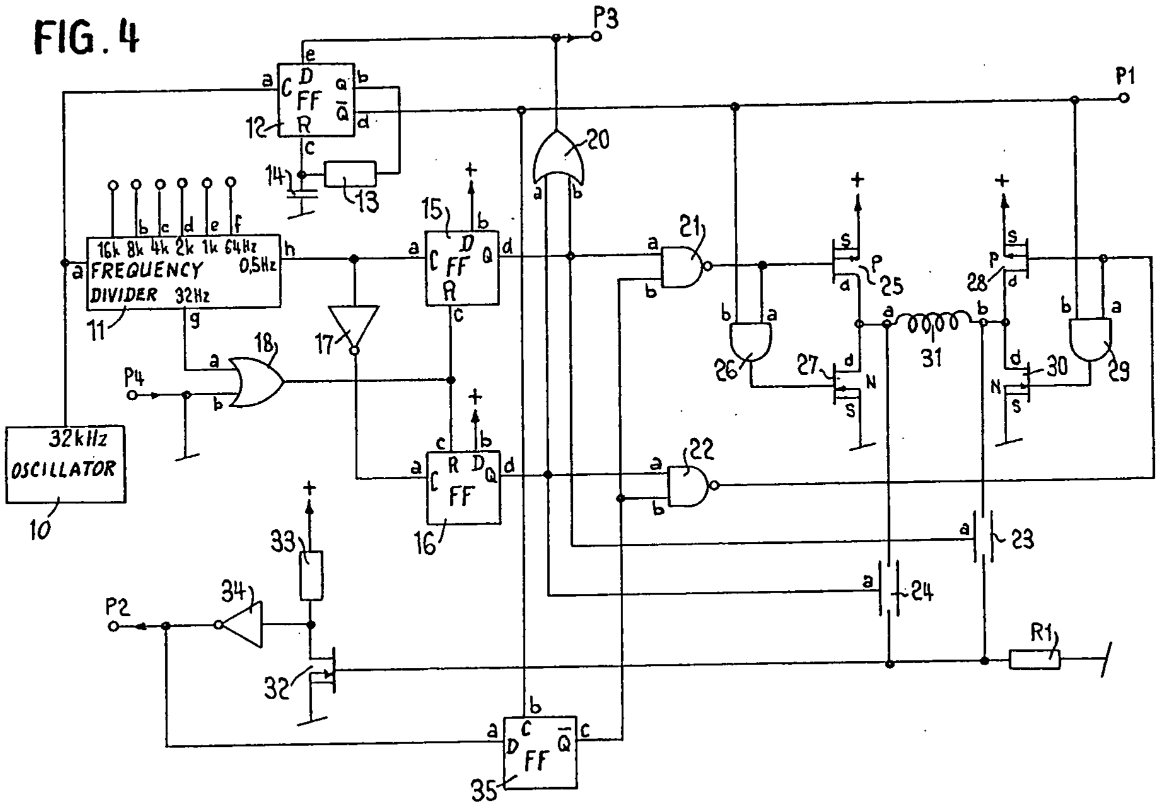

FIG.5

Element **64** is indeed a monostable flip-flop. The cited portion of the description states that the output of an AND gate is connected through an amplifier to the input of monostable flip-flop **64**. This is certainly evidence that **some** flip-flop circuit components may be modified or designed to operate as monostable circuit components. However, *Haubner* does not prove in any way that the specific D-type flip-flop of *van Driest* is monostable. The Examiner appears to be arguing that because **some** flip-flops may be modified or designed to operate as monostable circuit components, **all** flip-flops must necessarily be monostable, even flip-flops that are well known in

the art to be bistable. This is unquestionably untrue and only serves to prove that the specific teachings of *van Driest* fail to show a **functionally different** monostable circuit component.

The Final Office Action also argues that *Berney* (U.S. Patent No. 4,439,717) discloses a D-type flip-flop operating as a monostable circuit, as shown as element **12** of **Figure 4** and as described in col. 4, lines 10-27. **Figure 4** of *Berney* is reproduced as follows:

FIG. 4




The corresponding description in *Berney* states:

> **FIG. 4** shows by way of example the diagram of a control circuit of the device according to the invention, which makes it possible for the current in the coil to be maintained at a fixed value during the pulses for controlling the movement of the motor. A quartz oscillator **10** supplies a 32 kHz signal to the clock inputs a of a frequency divider **11** and to a D-type flip-flop **12** operating in a monostable mode. For that purpose, the output Q (b) of the flip-flop is connected by a resistor **13** to its reset input (c) and to a capacitor **14** which is connected to ground. Thus, whenever the flip-flop **12** goes to logic state "1", the capacitor **14** is charged through the resistor **13** and resetting occurs after a certain delay which is of very short duration (2µs for example). The flip-flop **12**

> therefore produces fine pulses of a duration of 2μs at a repetition frequency of 32 kHz when its input D (e) is at state "1".

*Berney*, col. 4, lines 11-27. Thus, in **Figure 4**, *Berney* clearly shows four D-type flip-flops **12**, **15**, **16**, and **35**. One of the D-type flip-flops **12** has a resistor **13** and capacitor **14** connected in such a way as to make the D-type flip-flop operate in a monostable mode. Thus, D-type flip-flops **15**, **16**, and **35** operate in bistable mode and D-type flip-flop would operate in bistable mode if not for resistor **13** and capacitor **14**. In other words, all four D-type flip-flops are, by definition, inherently bistable. *Berney* proves that some modification is necessary to make a bistable D-type flip-flop operate in a monostable mode. No such modification is made to the D-type flip-flop of *van Driest*; therefore, the D-type flip-flop of *van Driest* is unquestionably a bistable circuit component.

The Final Office Action further states that it would have been obvious to a person of ordinary skill in the art at the time of the invention that a D-type flip-flop can be considered a monostable circuit component, thus satisfying the limitations of the claims. Appellant respectfully disagrees. What a D-type flip-flop **can** be is not at question. In order to establish a *prima facie* case of anticipation, the Examiner must show that the D-type flip-flop is **necessarily** a monostable circuit component, particularly as arranged in the claims. To the contrary, a person of ordinary skill in the art would easily recognize that a D-type flip-flop is, by definition, a bistable circuit component.

Since claims 2, 3, and 7 depend from claim 1, the same distinctions between *van Driest* and the invention recited in claim 1 apply for these claims. Additionally, claims 2, 3, and 7 recite other additional combinations of features not suggested by the reference. Therefore, Appellant respectfully requests that the rejection of claims 1-3 and 7 under 35 U.S.C. § 102 not be sustained.

### IA. <u>35 U.S.C. § 102, Alleged Anticipation of Claim 7</u>

More particularly, claim 7 recites, "wherein at least one of the first monostable circuit component and the second monostable circuit component are one-shot circuit components." The Office Action dismisses this feature by baldly concluding that a data flip-flop is a one-shot. Appellant respectfully disagrees. With respect to monostable multivibrators, *The Art of*

*Electronics*, by Paul Horowitz and Winfield Hill, states:

> The monostable multivibrator, or "one-shot" (emphasis on the word "one"), is a variation of the flip-flop (which is sometimes called a bistable multivibrator) in which the output of one of the gates is capacitively coupled to the input of the other gate. The result is that the circuit sits in one state. If it is forced to the other state by a momentary input pulse, it will return to the original state after a delay time determined by the capacitor value and the circuit parameters (input current, etc.).

See attached excerpt. Therefore, as clearly recognized in the art, a monostable multivibrator is referred to as a one-shot largely because a monostable circuit holds only one state stable. A D-type flip-flop is bistable; therefore, a D-type flip-flop is not equivalent to a monostable circuit component or a one-shot, as alleged in the Office Action. The applied reference fails to teach or fairly suggest each and every claim limitation. Therefore, *van Driest* does not anticipate claim 7.

Furthermore, *van Driest* does not teach, suggest, or give any incentive to make the needed changes to reach the presently claimed invention. *Van Driest* actually teaches away from the presently claimed invention because it teaches bistable circuit components, as opposed to a first monostable circuit component and a second monostable circuit component, as in the presently claimed invention.

## II. <u>35 U.S.C. § 103, Alleged Obviousness of Claim 4</u>

The Final Office Action rejects claim 4 under 35 U.S.C. § 103 as being unpatentable over *van Driest* in view of *Kobayashi* (US Patent No. 6,028,461). This rejection is respectfully traversed.

The Final Office Action acknowledges that *van Driest* does not teach or suggest an OR-gate logical operator to compare the output of the first monostable circuit component and the output of the second monostable circuit component. While OR gates may be generally known in the art, and *Kobayashi* does indeed teach an OR gate as part of a phase comparison circuit, the prior art, when considered as a whole, fails to teach or suggest an OR-gate logical operator being used to compare the output of a first monostable circuit component and the output of a second monostable circuit component. In fact, *Kobayashi* also fails to teach or suggest a monostable circuit component. Therefore, *Kobayashi* does not cure the deficiencies of *van Driest*. At best, *Kobayashi* suggests that an OR gate may be used as part of phase compare logic **86** in *van*

*Driest*. However, a combination of *van Driest* and *Kobayashi* would not form the presently claimed invention, because neither reference teaches or fairly suggests a monostable circuit component in any form.

Therefore, Appellant respectfully requests that the rejection of claim 4 under 35 U.S.C. § 103 not be sustained.

## III. 35 U.S.C. § 103, Alleged Obviousness of Claims 10, 35, and 36

The Final Office Action rejects claims 10, 35, and 36 under 35 U.S.C. § 103 as being unpatentable over *van Driest* in view of *Park* (US Patent No. 5,880,898). This rejection is respectfully traversed.

The Final Office Action acknowledges that *van Driest* does not teach or suggest an equalizer to equalize the received input data. While data equalizers may be generally known in the art, the prior art, when considered as a whole, fails to teach or suggest an equalizer that provides an equalized data signal to the input of a first monostable circuit component and the input of a second monostable circuit component, as recited in claim 3, upon which claim 10 depends. In fact, *Park* also fails to teach or suggest a monostable circuit component. Therefore, *Park* does not cure the deficiencies of *van Driest*. At best, *Park* suggests that the glitch error removal portion of *Park* may provide an equalized data input to received data line **40** of *van Driest*. However, a combination of *van Driest* and *Park* would not form the presently claimed invention, because neither reference teaches or fairly suggests a monostable circuit component in any form.

Independent claim 35 recites subject matter addressed above with respect to claim 1 and 10 and is allowable for at least the same reasons. Since claim 36 depends from claim 35, the same distinctions between *van Driest* and *Park* and the invention recited in claim 35 applies for this claim. Additionally, claim 36 recites other additional combinations of features not suggested by the reference. Therefore, Appellant respectfully requests that the rejection of claims 10, 35, and 36 under 35 U.S.C. § 103 not be sustained.

## IV. 35 U.S.C. § 103, Alleged Obviousness of Claim 12

The Final Office Action rejects claim 12 under 35 U.S.C. § 103 as being unpatentable

over *van Driest* in view of *Park* and further in view of *Streckmann et al.* (US Patent No. 4,535,299). This rejection is respectfully traversed.

The Office Action acknowledges that the proposed combination of *van Driest* and *Park* does not teach or suggest a resistive-capacitive differentiator. While resistive-capacitive differentiators may be generally known in the art, the prior art, when considered as a whole, fails to teach or suggest a resistive-capacitive differentiator as part of an equalizer that provides a differentiated data signal to the input of a first monostable circuit component and the input of a second monostable circuit component, as recited in claims 3 and 10 upon which claim 12 depends. In fact, *Streckmann* also fails to teach or suggest a monostable circuit component. Therefore, *Streckmann* does not cure the deficiencies of *van Driest* and *Park*. At best, *Streckmann* suggests that the differentiator of *Streckmann* may be used in place of the differentiator **61** of *Park*. However, a combination of *van Driest*, *Park*, and *Streckmann* would not form the presently claimed invention, because none of the applied references teaches or fairly suggests a monostable circuit component in any form.

Therefore, Appellant respectfully requests that the rejection of claim 12 under 35 U.S.C. § 103 not be sustained.

## V. <u>35 U.S.C. § 103, Alleged Obviousness of claim 37</u>

The Office Action rejects claim 37 under 35 U.S.C. § 103 as being unpatentable over *van Driest* in view of *Park* and further in view of *Kobayashi*. This rejection is respectfully traversed.

The Office Action acknowledges that *van Driest* and *Park* fail to teach or suggest an OR-gate logical operator to compare the output of the first monostable circuit component and the output of the second monostable circuit component. While OR gates may be generally known in the art, and *Kobayashi* does indeed teach an OR gate as part of a phase comparison circuit, the prior art, when considered as a whole, fails to teach or suggest an OR-gate logical operator being used to compare the output of a first monostable circuit component and the output of a second monostable circuit component. In fact, *Kobayashi* also fails to teach or suggest a monostable circuit component. Therefore, *Kobayashi* does not cure the deficiencies of *van Driest* and *Park*. At best, *Kobayashi* suggests that an OR gate may be used as part of phase compare logic **86** in *van Driest*. However, a combination of *van Driest*, *Park*, and *Kobayashi* would not form the

presently claimed invention, because none of the applied references teaches or fairly suggests a monostable circuit component in any form.

Therefore, Appellant respectfully requests that the rejection of claim 37 under 35 U.S.C. § 103 not be sustained.

## CONCLUSION

In view of the above, Appellant respectfully submits that claims 1-4, 7, 10, 12, and 35-37 are allowable over the cited prior art and that the application is in condition for allowance. Accordingly, Appellant respectfully requests the Board of Patent Appeals and Interferences to not sustain the rejections set forth in the Final Office Action.

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## APPENDIX OF CLAIMS

The text of the claims involved in the appeal reads:

1. A signal recovery method for a self-clocked transmission system, comprising the steps of:

inputting a received data signal to both a first monostable circuit component and a second monostable circuit component;

generating a first output signal from the first monostable circuit component and a second output signal from the second monostable circuit component;

comparing the first output signal and the second output signal to each other using a first logical operator; and

outputting a compared output signal based on the comparison.

2. The method of claim 1, wherein the signal recovery consists of at least one of a clock signal and a data signal.

3. The method of claim 1, wherein the received data signal is at least one of a processed equalized data signal and a processed unequalized data signal.

4. The method of claim 1, wherein the first logical operator is an OR-gate logical operator.

7. The method of claim 1, wherein at least one of the first monostable circuit component and the second monostable circuit component are one-shot circuit components.

10. The method of claim 3, wherein equalizing the inputted data signal includes;

differentiating the inputted data signal;

amplifying the differentiated data signal;

applying a sign element to the amplified data signal; and

decreasing the signed amplified data signal.

12. The method of claim 10, wherein differentiating the received data signal includes a resistive-capacitive differentiator.

35. A signal recovery system for a self-clocked transmission system, comprising:

an equalizer, wherein the equalizer has at least one output port;

a first monostable circuit component having at least two input ports and two output ports, wherein the output port of the equalizer is connected to a first input port of the first monostable circuit component;

a second monostable circuit component having at least two input ports and two output ports, wherein the output of the equalizer is connected to a first input port of the second monostable circuit component; and

a first logical operator having at least two input ports and one output port, wherein a first output port of the first monostable circuit component is connected to a first input port of the first logical operator and a first output port of the second monostable circuit component is connected to the second input port of the first logical operator.

36. The system of claim 35, further comprising:

a data flip-flop circuit component having a data input port, a clock input port and a complementary clock input port and having an output port and a complementary output port, wherein the output port of the first logical operator is connected to the clock input port of the data flip-flop circuit component; and

a constant signal source, wherein the constant signal source is connected to the complementary clock input port of the data flip-flop circuit component.

37. The system of claim 35, wherein the first logical operator is an OR-gate.

## EVIDENCE APPENDIX

The following dictionary definitions and excerpts were presented and entered as part of the Response to Office Action filed April 2, 2004:

*IBM Dictionary of Computing*, definition of "bistable" on page 55, definition of "bistable trigger circuit" on page 55, definition of "monostable" on page 368.

"4013 D-type flip-flops" from http://www.doctronics.co.uk/4013.htm.

Wikipedia definition for "flip flop" from http://en.wikipedia.org/wiki/Flip-flop.

*The Art of Electronics*, by Paul Horowitz and Winfield Hill, page 517.

Copies of these definitions and excerpts are attached.

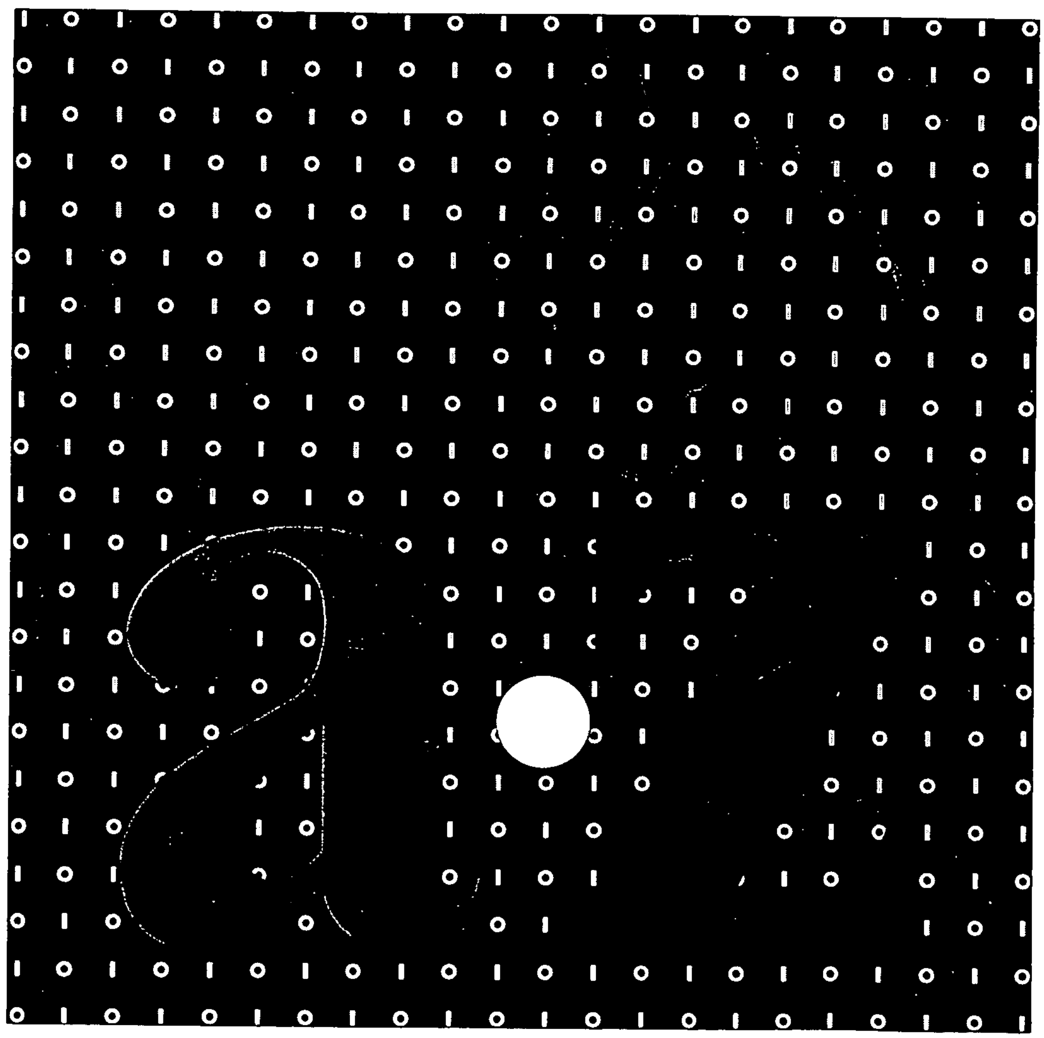
## RELATED PROCEEDINGS APPENDIX

There are no related proceedings.

# Dictionary of Computing

SC20-1699-8

## Information Processing, Personal Computing, Telecommunications, Office Systems, IBM-specific Terms



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While the Author and Publisher of this book have made reasonable efforts to ensure the accuracy and timeliness of the information contained herein, neither the Author nor the Publisher shall have any liability with respect to loss or damage caused or alleged to be caused by reliance on any information contained herein.

# Preface

This dictionary includes terms and definitions from:

- The *American National Standard Dictionary for Information Systems*, ANSI X3.172-1990, copyright 1990 by the American National Standards Institute (ANSI). Copies may be purchased from the American National Standards Institute, 11 West 42nd Street, New York, New York 10036. Definitions are identified by the symbol (A) after the definition.
- The ANSI/EIA Standard -- 440-A, *Fiber Optic Terminology*. Copies may be purchased from the Electronic Industries Association, 2001 Pennsylvania Avenue, N.W., Washington, DC 20006. Definitions are identified by the symbol (E) after the definition.
- The *Information Technology Vocabulary*, developed by Subcommittee 1, Joint Technical Committee 1, of the International Organization for Standardization and the International Electrotechnical Commission (ISO/IEC JTC1/SC1). Definitions of published parts of this vocabulary are identified by the symbol (I) after the definition; definitions taken from draft international standards, committee drafts, and working papers being developed by ISO/IEC JTC1/SC1 are identified by the symbol (T) after the definition, indicating that final agreement has not yet been reached among the participating National Bodies of SC1.
- Information for IBM products announced since the previous (1987) edition of the IBM *Dictionary of Computing*, SC20-1699-7, which this dictionary replaces. Definitions that are specific to IBM products are so labeled, for example, "In SNA," or "In VM." The complete names of IBM systems and hardware products are listed in "Nomenclature of IBM Systems and Machines" on page 635. Names of IBM software products are given in the *IBM Software Directory*, GB21-9949.

See "New in this Edition" on page viii for specific sources of new material.

The dictionary provides a comprehensive reference for anyone who uses, maintains, or has an interest in information processing systems, communication products and facilities, personal computers and office systems. Some of these terms may have other meanings in other contexts, or among people not familiar with the use of these terms in information processing, communication, personal computers, and office systems. With the exception of common electrical and metric measures, the dictionary excludes terms that are defined in nontechnical dictionaries and that have no special meaning in information processing.

## Sequence of Entries

For clarity and consistency of style, this dictionary uses the same method of arranging entries as that used in *Webster's Ninth New Collegiate Dictionary*, Merriam-Webster, Inc., Springfield, Massachusetts, 1984, and in the *American National Standard Dictionary for Information Systems*, American National Standards Institute, Inc., New York, New York, 1990. The sequence of entries is determined alphabetically on a letter-by-letter basis. Only the letters of the alphabet are used to determine sequence; special characters and spaces between words are ignored.

## Organization of Entries

Each entry consists of a single-word or multiple-word term or the abbreviation or acronym for a term, followed by a commentary. A commentary includes one or more items (definitions or references) and is organized as follows:

- An item number, if the commentary contains two or more items.
- A usage label, indicating the area of application of the term, for example, "In programming," or "In SNA."
- A descriptive phrase, stating the basic meaning of the term. The descriptive phrase is assumed to be preceded by "the term is defined as ..." The part of speech being defined is indicated by the opening words of the descriptive phrase: "To ..." indicates a verb and "Pertaining to ..." indicates a modifier. Any other wording indicates a noun or noun phrase.
- Annotative sentences, providing additional or explanatory information.
- References, directing the reader to other entries or items in the dictionary.
- A source label, for example, (A), (E), (I), or (T), that follows the definition and identifies the originator of the definition. Definitions without source labels are IBM definitions.

**biquinary code**. A notation in which a decimal digit n is represented by the pair of numerals a, b, where a equals 0 or 1, b equals 0, 1, 2, 3, or 4, and the sum of 5a + b is equal to n. (T) (A)

**BISAM**. Basic indexed sequential access method.

**BIST**. Built-in self-test.

**bistable**. Pertaining to a device capable of assuming either of two stable states. (A)

**bistable circuit**. See bistable trigger circuit.

**bistable trigger circuit**. (1) A trigger circuit that has two stable states. (T) (2) Synonymous with flip-flop.

**BISYNC**. Binary synchronous.

**bit**. (1) Either of the digits 0 or 1 when used in the binary numeration system. Synonymous with binary digit. (T) (2) Deprecated term for binary element, shannon. (3) See check bit, D-bit, information bits, M-bit, parity bit, Q-bit, qualifier bit, redundancy check bit, sign bit, sticky bit.

**bit block**. In MSP/7, a storage area defined by a BIT macroinstruction to identify a program, task, or interrupt fan routine. It is accessed by $FAN while processing an interrupt fan routine.

**bit-block transfer (bitblt)**. (1) Transfer of a rectangular array of bit-map data. (2) In the AIX* operating system, the movement of a binary image (a bitmap or pixmap) by specifying the lower-left and upper-right corners of the image and the destination address.

**bit BLT**. Bit block transfer.

**bitblt**. Bit-block transfer.

**bit clocking**. In an EIA-232 interface, the field that indicates which piece of equipment, either the modem or the computer, provides the clock signal for synchronized data transactions.

**bit comparison**. In PL/I, a left-to-right, bit-by-bit comparison of binary values. See also arithmetic comparison, character comparison.

**[illegible] configuration**. The order for encoding the bits of infor-[illegible]ation that define a character. (T) (A)

**[illegible] constant**. In PL/I, either a series of binary numbers [illegible]closed in apostrophes and followed immediately by B or [illegible] or a series of hexadecimal numbers enclosed in apos-[illegible]phes and followed immediately by B4. Contrast with [illegible]acter constant.

**[illegible]ensity**. A measure of the number of bits recorded per [illegible] length or area. Synonymous with recording density.

**[illegible]ror rate (BER)**. In fiber optics, a comparison of the [illegible] of bits received incorrectly to the total number of [illegible]smitted. The BER relates directly to receiver sensitivity, transmitter power output, pulse dispersion, and total link attenuation.

**bit field**. A member of a structure or union that contains one or more named bits.

**bit gravity**. In AIX* Enhanced X-Windows, the attraction of window contents for a location in a window. When a window is resized, its contents can be relocated. The server can be requested to relocate the previous contents to a region of the window.

**bit map**. (1) A coded representation in which each bit, or group of bits, represents or corresponds to an item; for example, a configuration of bits in main storage in which each bit indicates whether a peripheral device or a storage block is available or in which each group of bits corresponds to one pixel of a display image. (2) A pixmap with a depth of one bit plane. See also stipple. (3) In DPCX, a control record that describes 1432 256-byte blocks of disk storage.

**bit map display**. A display on which characters or images are generated by writing the bit pattern to be displayed into the associated storage, each bit of which is mapped to a pixel on the display surface. (T)

**bit-map graphics**. A form of graphics in which all points on the display are directly addressable.

**bit-mapped display**. A display with a display adapter that has a hardware representation of each separately addressable point on the display. The hardware representation can be processor memory or adapter memory. See all points addressable display.

**bit plane**. In computer graphics, one bit of color information per pixel on the display. Thus, an eight bit-plane system allows 2 to the eighth power different colors to be displayed at each pixel. See also overlay planes.

**bit position**. (1) A character position in a word in a binary notation. (T) (2) A digit position in a binary number.

**bit rate**. The speed at which bits are transmitted, usually expressed in bits per second. See also baud.

**bits per character**. The number of bits in a data character.

**31-bit storage addressing**. The storage address structure available in an MVS/XA* operating system.

**bit stream**. A binary signal without regard to grouping by character.

**bit string**. A string consisting solely of bits. (I) (A)

**bit value**. In PL/I, a sequence of binary numbers stored in consecutive bits.

**BIU**. Basic information unit.

**BIU segment**. In SNA, the portion of a basic information unit (BIU) that is contained within a path information unit (PIU). It consists of either a request/response header (RH) followed

patterns, such as a sampling frequency and a correct frequency, are superimposed. The moire pattern is an alias frequency. See also aliasing.

**moistening pressure roller**. In a duplicator, a roller that applies pressure to the surface of the moistening roller to transfer the paper through the damping system. (T) Synonymous with conveying roller.

**moistening roller**. In a duplicator, a roller that transfers moisture from the damping pad to the surface of the copy paper. (T)

**MOM**. Monitor mode.

**monadic Boolean operator**. A Boolean operator having only one operand; for example, NOT. (A)

**monadic operation**. An operation with one and only one operand. (I) (A) Synonymous with unary operation.

**monadic operator**. An operator that represents an operation on one and only one operand. (I) (A) Synonymous with unary operator.

**monitor**. (1) A device that observes and records selected activities within a data processing system for analysis. Possible uses are to indicate significant departure from the norm, or to determine levels of utilization of particular functional units. (T) (2) Software or hardware that observes, supervises, controls, or verifies operations of a system. (A) (3) Synonym for video display terminal. (4) In the IBM* Token-Ring Network, the function required to initiate the transmission of a token on the ring and to provide soft-error recovery in case of lost tokens, circulating frames, or other difficulties. The capability is present in all ring stations. (5) See video monitor.

**monitoring program**. Synonym for monitor program.

**monitor mode**. (1) A mode of the network control program in which the host is immediately notified when an attention, disconnect, or unusual status occurs on a designated line. (2) In an 8100 loop, a secondary station operating mode in which the station is receiving and analyzing loop traffic, but is not inserted into the loop. See also inserted mode. (3) In System/38, the mode during which a communication adapter searches for BSC synchronization characters. (4) In the AIX* operating system, a mode in which an application program can directly access the display adapter.

**monitor printer**. A device that prints all messages transmitted over the circuit to which it is connected.

**monitor program**. A computer program that observes, regulates, controls, or verifies the operations of a data processing system. (I) (A) Synonymous with monitoring program.

**monitor task**. In DPCX with the program execution monitor, the task in which the system debugging function is used to monitor a program or subtask.

**monitor terminal**. In DPCX with the program execution monitor, the terminal from which the system debugging function is selected and from which a task or subtask is initiated for monitoring. The monitor terminal is used to enter commands that control the execution of the test task.

**monochrome**. Consisting of a single color.

**monochrome display**. A display device that presents display images in only one color. Contrast with color display. See also gray scale.

**monolithic integrated circuit**. A type of integrated circuit whose substrate is an active material, such as the semiconductor silicon.

**monolithic storage**. Storage made up of monolithic integrated circuits.

**monolithic technology**. A technology in which all electronic components of a circuit, such as transistors, diodes, resistors, and capacitors, are integrated into one chip; for example, MST.

**monomode optical fiber**. Synonym for single-mode optical fiber.

**monospacing**. A method of spacing in which the space between characters does not vary. Contrast with proportional spacing.

**monostable**. Pertaining to a device that has one stable state. (A)

**monostable circuit**. Synonym for monostable trigger circuit.

**monostable trigger circuit**. A trigger circuit that has one stable state and one unstable state. (I) (A) Synonymous with monostable circuit.

**Monte Carlo method**. A method of obtaining an approximate solution to a numerical problem by the use of random numbers; for example, the random walk method, or a procedure using a random number sequence to calculate an integral. (I) (A)

**More**. In SAA* Basic Common User Access* architecture, scrolling information that indicates to a user that more information is available by scrolling. See scrolling arrows.

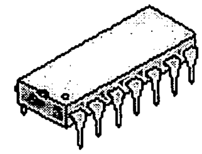
**more-data bit**. See M-bit.

**MORE screen status**. For a display terminal used as a virtual console under VM, an indicator located in the lower right of the screen that notifies the user that the display screen is full, but that there is more data to be displayed. After 60 seconds, the screen is automatically erased and the next image is displayed.

**MOS**. Metal oxide semiconductor. A type of semiconductor used in devices such as field-effect transistors. See also CMOS, HMOS, NMOS, PMOS.

**mosaic**. Deprecated term for aggregation.

# 4013 Dual D-type flip-flops



Technology: CMOS | Power supply: 3-15 V | 14-pin DIL

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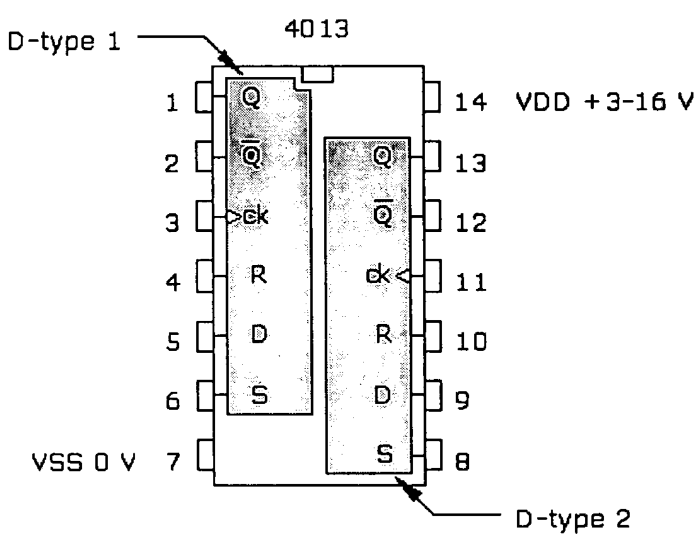
## Pin connections



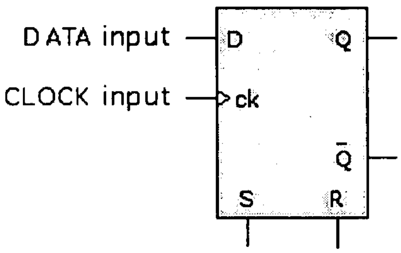

*The 4013 has two D-type flip-flops, which you can use independently*

Up

## About D-type flip-flops

A D-type flip-flop, also called a **D-type bistable**, is a subsystem with **two stable states**. Using appropriate input signals, you can trigger the flip-flop from one state to the other.

The diagram below shows the input and output connections of a single D-type bistable:

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$Q$ and $\overline{Q}$ are the **outputs** of the bistable. The logic states of the outputs are always opposite.

The bistable is **SET** when $Q = 1$ and $\overline{Q} = 0$, and **RESET** when $Q = 0$ and $\overline{Q} = 1$.

---

The D-type has four **inputs**. These are:

- **DATA** input: This is connected either to a LOW voltage, logic 0, or to a HIGH voltage, logic 1.
- **CLOCK** input: The triangle, ck, next to the CLOCK input shows that it is **edge-triggered**, that is, it responds to sudden changes in voltage, but *not* to slow changes or to steady logic levels. The CLOCK input of the 4013 D-type bistable is **rising-edge triggered**, meaning that it responds *only* to a sudden change from LOW to HIGH.

  Usually, the CLOCK input is connected to a subsystem which delivers pulses. To test the 4013, you will need to build an astable.

- **SET** input: The SET input is normally held LOW. When it is pulsed HIGH, the outputs of the bistable are forced immediately to the SET state, $Q = 1$, $\overline{Q} = 0$.
- **RESET** input: The RESET input is normally held LOW. When it is pulsed HIGH, the outputs of the bistable are forced immediately to the RESET state, $Q = 0$, $\overline{Q} = 1$

---

To explain the behaviour of the D-type bistable, you can learn to say that:

**The logic state at the DATA input is transferred to the $Q$ output on the rising edge of the**

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# Flip flop

(Redirected from Flip-flop)

In electronics and computing, the **flip-flop** or *bistable multivibrator* is an electronic circuit which in its simplest form consists of two transistors (or vacuum tubes) connected in such a way that the circuit can be in one of two stable conditions. A trigger applied at an appropriate point can cause the circuit to flip from one state to the other. A trigger at another point can cause the circuit to flop back to the other state. It is also possible to arrange it so that repeated triggers at one point cause it to change state back and forth.

See also: monostable multivibrator, astable multivibrator.

The first electronic flip-flop was invented in 1919 by W. H. Eccles and F. W. Jordan. It was initially called the *Eccles-Jordan trigger circuit*.

**Table of contents** [hide]



## Types of flip-flops

### T flip-flop

One way of changing the state is to have the flip-flop's state invert when a clock signal changes state. Usually they change only when the clock moves in a particular direction, e.g. low (ground) to high (for example 5 volts). This is called a *T-type* (for "toggle") flip-flop. Several T flip-flops can be connected together to form a *divide by N* counter.

Characteristic equation: $Q_{next} = T \oplus Q = T\overline{Q} + \overline{T}Q$

### S-R flip-flop

A "set/reset" flip-flop in which activating the "set" ("S") input will switch it to one stable state and activating the "reset" ("R") input will switch it to the other state.

The outputs of a basic S-R flip-flop change whenever its R or S inputs change

appropriately. A clocked S-R flip-flop has an extra clock input which enables or disables the other two inputs. When they are disabled the outputs remain constant.

If one connects two clocked S-R flip-flops so that the Q and /Q outputs of the first (or "master") flip-flop drive the S and R inputs of the second (or "slave") flip-flop, and the slave's clock input is driven with an inverted version of the master's clock, then this is an edge-triggered R-S flip-flop. The external R and S inputs of this device are latched on one edge (transition) of the clock (e.g. the falling edge) and the outputs will only change on the next opposite (rising) edge.

If both R and S inputs are active (when enabled), a race condition occurs and the outputs will be in an indeterminate state. A J-K flip-flop avoids this possibility.

### J-K flip-flop

A third type of flip-flop is composed of a pair of *S-R* flip-flops connected in series as a Master and Slave. The Master section receives the inputs and is gated by a clock while the Slave section is gated by an inversion of that clock. The Slave's outputs are cross-coupled back to the input gates of the Master as well as being the outputs. This is called an *J-K* flip-flop. By connecting its *J* and *K* inputs in various different ways this versatile flip-flop could be configured to toggle, store data, and perform many other functions.

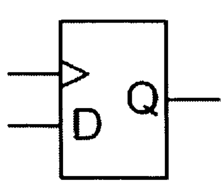
A J-K flip-flop operates as follows:

- If both inputs are logic 0, the flip-flop remains in the same state as it was before the clock pulse occurred.
- If both inputs are logic 1, the flip-flop changes state whenever the edge of a clock pulse occurs (T flip-flop behaviour).
- If one input (J or K) is at logic 0, and the other is at logic 1, then the output is set or reset (by J and K respectively).

Characteristic equation: $Q_{next} = J\overline{Q} + \overline{K}Q$

### D flip-flop

A fourth type records an input's state (the data) when a clock is pulsed. This is called a *D-type* (for "data") flip-flop. The D is also said to be for "delay", since the data arrives at the output one clock cycle after it arrives at the input.




Left: A circuit symbol for a D-type flip-flop, where > is the clock input, D is the data input and Q is the stored data output.

Characteristic equation: $Q_{next} = D$

# THE ART OF ELECTRONICS

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Paul Horowitz HARVARD UNIVERSITY

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## MONOSTABLE MULTIVIBRATORS

The monostable multivibrator, or "one-shot" (emphasis on the word "one"), is a variation of the flip-flop (which is sometimes called a bistable multivibrator) in which the output of one of the gates is capacitively coupled to the input of the other gate. The result is that the circuit sits in one state. If it is forced to the other state by a momentary input pulse, it will return to the original state after a delay time determined by the capacitor value and the circuit parameters (input current, etc.). It is very useful (some would say *too* useful!) for generating pulses of selectable width and polarity. Making one-shots with gates and *RC*s is tricky, and it depends on the details of the gate's input circuit, since, for instance, you wind up with voltage swings beyond the supply voltages. Rather than encourage bad habits by illustrating such circuits, we will just treat the one-shot as an available functional unit. In actual circuits it is best to use a packaged one-shot; you construct your own only if absolutely necessary, e.g., if you have a gate available and no room for an additional IC package (even then, maybe you shouldn't).

### 8.20 One-shot characteristics

#### *Inputs*

One-shots are triggered by a rising or falling edge at the appropriate inputs. The only requirement on the triggering signal is that it have some minimum width, typically 25ns to 100ns. It can be shorter or longer than the output pulse. In general, several inputs are provided so that several signals can trigger the one-shot, some on positive edges and some on negative edges (remember, a negative edge means a HIGH-to-LOW transition, not a negative polarity). The extra inputs can also be used to inhibit triggering. Figure 8.64 shows four examples.

Each horizontal row of the table represents a valid input triggering transition. For example, the '121 will trigger when one of the $A$ inputs makes a HIGH-to-LOW transition, if the $B$ input and the other $A$ input are both HIGH. The '4538 is a dual CMOS monostable with OR gating at the input; if only one input is used, the other must be disabled, as shown. The '121 has three inputs, with a combination of OR and AND gating (and triggering), as shown. Its $B$ input is a Schmitt trigger, more forgiving with slowly rising or noisy input signals. This monostable also includes a not-too-good internal timing resistor you can use instead of $R$, if you're feeling lazy. The '221 is a dual '121; CMOS users can get only the dual version. The popular '123 is a dual monostable with AND input gating; unused inputs must be enabled. Note particularly that it triggers when RESET is disabled if both trigger inputs are already asserted. This is not a universal property of monostables, and it may or may not be desirable in a given application (it's usually not). The '423 is the same as the '123, but without this "feature."

When drawing monostables in a circuit diagram, the input gating is usually omitted, saving space and creating a bit of confusion.

#### *Retriggerability*

Most monostables, e.g., the 4538, '123, and '423 mentioned earlier, will begin a new timing cycle if the input triggers again during the duration of the output pulse. They are known as retriggerable monostables. The output pulse will be longer than usual if they are retriggered during the pulse, finally terminating one pulse width after the last trigger. The '121 and '221 are nonretriggerable; they ignore input transitions during the output pulse. Most retriggerable one-shots can be connected as nonretriggerable one-shots.

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